E-PHEMT, Single Supply, High Efficient Power Amplifiers for GSM and DCS Applications

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ABSTRACT **This paper presents power amplifier MMICs for GSM and DCS applications using a newly developed 0.5um enhancement mode power PHEMT process. An Automatic Bias Control (ABC) circuit is implemented on-chip to achieve high PAE. A Voltage Variable Attenuator (VVA) is also designed and fabricated on-chip to adjust the input power level and the overall gain. Under a low single supply voltage of 3.2V the GSM PA provides 35 dBm output power with 55% PAE, and the DCS PA delivers 33dBm with 40% PAE. Both chips are housed in 20-pin 4mm´4mm Miniature Leadless Packages (MLP).**

I. INTRODUCTION

In Today's handset phone systems, power amplifiers are critical devices, which determine important system parameters such as talk time, standby time, overall cost, and size. A handset requires the RF PA to offer high power added efficiency to achieve a long talk time. In addition, a single low voltage power supply PA is desirable, because it eliminates the need for a negative power supply, therefore reducing the overall size and system complexity. Meanwhile, if the drain current leakage is kept adequately low while in the standby condition, no drain switch will be required to shut off the PA completely. For these reasons, an enhancement mode PHEMT (E-PHEMT) PA [1][3] offers an attractive solution for the handset applications.

II. E-PHEMT PROCESS

A 0.5um enhancement mode power PHEMT process has recently been developed at Alpha Industries for handset PA applications. The E-PHEMT epi-structure and recess etch conditions were optimized to keep Idss at minimal levels, while maintaining Imax and transconductance high enough to achieve adequate RF performance.

Fig. 1 shows pulsed transfer IV characteristics of a 4mm E-PHEMT device. The E-PHEMT device has Idss of approximately 8uA/mm, Imax=370mA/mm, Vp=0.3V, and Gm=500mS/mm at Vds=2V.

Load pull measurements have been performed on different periphery PHEMT devices. The typical Pout and PAE versus Pin obtained on a 40×100um FET is shown in Fig. 2. Terminal impedances have been tuned for optimal power and PAE at Ids=100mA, and Vds=3.2V. An efficiency of 74% was achieved with an output power 27.5dBm at 900MHz, which corresponds to 140mW/mm power density. The Breakdown voltage was greater than 16V for the E-PHEMT device at Ig=0.5mA/mm, and the small signal gain of the device was 27dB.

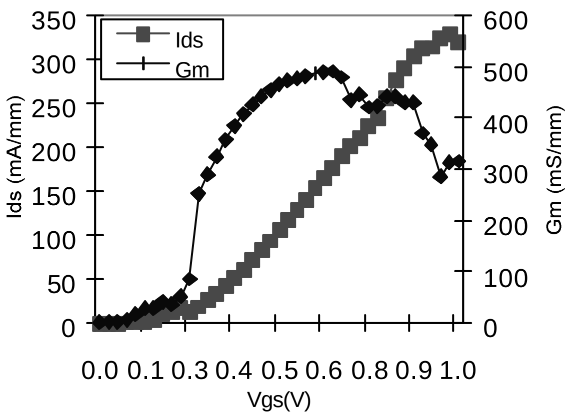

Fig. 1. Pulsed IV characteristics of 4 mm E-PHEMT device on-wafer measurement results at Vds=2V

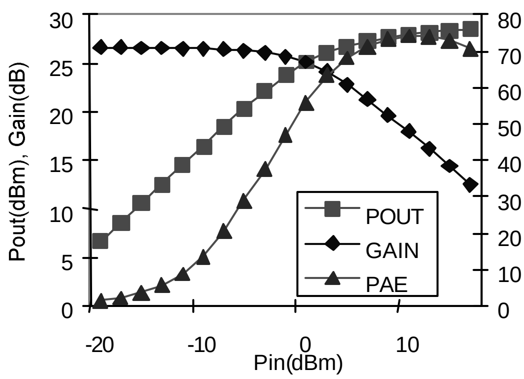

Fig. 2. On-wafer load pull measurement results for a 4mm PHEMT device under Ids=100mA and Vds=3.2V at 900 MHz

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II. PA CIRCUITS DESIGN

E-PHEMT MMIC PAs for GSM and DCS applications were developed at Alpha Industries. Targeted output power for the GSM PA in a 50Ù system was 34.4dBm, and for the DCS PA it was 32.2dBm, both using a 3.2V power supply and a 5dBm input power level. Considering the high gain requirement of greater than 30dB at full output power levels, a three stages amplifier topology was employed. The design cycle began with on-wafer load-pull characterization, which provided an estimate of the required FET size, bias conditions, gain, power, and PAE under the proper impedance conditions. Next, load-pull simulation was carried out based on the extracted large signal FET model[1] to finalize the optimized impedances for each stage FET device. Since GSM and DCS PAs are operated using a constant envelope modulation, the PAs are designed to operate at the deep saturated condition to achieve high power added efficiency. Matching circuits were then synthesized with the input and inter-stage matching circuits realized on-chip. The output matching circuit was realized on a printed circuit board to reduce power loss by taking advantage of high Q ceramic components. The package parasitics were included in the circuit design from the very beginning and bond wire inductances were used to help implement the matching networks. An RC feedback loop is employed around the first stage to ensure the stability of the PAs. The schematic circuit for GSM and DCS PAs is shown in Fig. 3. In front of the three-stage PA, a Voltage Controlled Variable Attenuator (VVA) was also designed and implemented on-chip. This VVA is used to control the input power level. In addition, an Automatic Bias Control (ABC) circuit was designed and implemented on-chip.

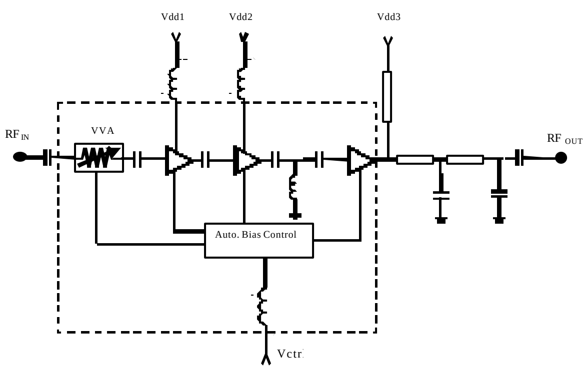

Fig. 3. A block diagram illustrating the structure of the presented three-stage power amplifier

III. MEASUREMENT RESULTS

The performance of GSM and DCS power amplifiers were investigated using evaluation boards where the output matching circuit was implemented using surface mount components and adjusting for optimized performance. Typical performance of a GSM PA with Vdd = 3.2V versus input power is shown in Fig. 4. It is found that the gain is as high as 39dB at low power level and reduced to 30dB at about +35dBm with 55% PAE. Input return loss (RL) is less than -10dB over the whole input power range. By sweeping the power control voltage from 0 to 2V with Pin=5dBm, the output power of the GSM PA was changed from –8dBm to +35dBm (Fig. 5). This corresponds to a dynamic range for power control of about 43dB.

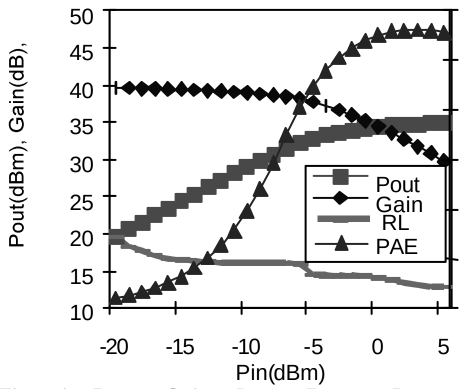

Fig. 4. Pout, Gain, Input Return Loss and PAE versus Pin for GSM power amplifier under 3.2V at 900 MHz

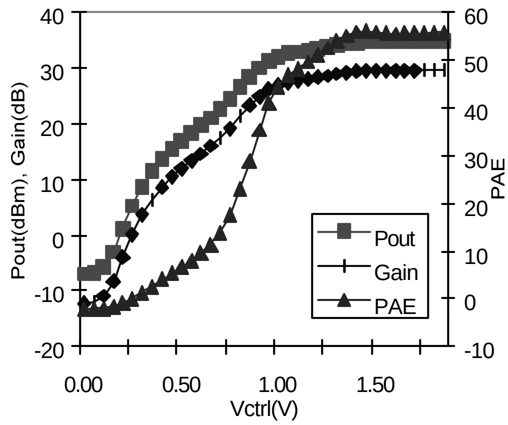

Fig. 5. Pout, Gain and PAE as a function of Power Control Voltage for GSM power amplifier under 3.2V and Pin=5dBm at 900MHz

The DCS power amplifier operating at 1800MHz was also evaluated. Typical performance of the DCS PA with Vdd= 3.2V versus input power is shown in Fig. 6. The DCS PA delivers +33dBm output power with 40% PAE at 1800MHz with the input power level at 5dBm. Input return loss is less than -15dB over the whole power range, indicating an excellent input match achieved. By varying the control voltage from 0 to 2V at Pin =5dBm, the DCS PA output power can be changed from –12dBm to +33dBm, a 45dB dynamic range, as shown in Fig. 7. The VVA performance at GSM and DCS bands were also verified on-wafer to guarantee that the whole chip has excellent performance. As shown in Fig. 8, the maximum attenuation of the GSM and DCS VVAs are 25dB and 28dB respectively with the control voltage at 0V. The insertion loss of the GSM and DCS VVAs are about -2dB when the control voltage is set to 2V. The GSM and DCS amplifiers are housed in the 4×4mm miniature leadless plastic (MLP) package, MLP20. Fig. 9 shows the photograph of an assembled DCS PA.

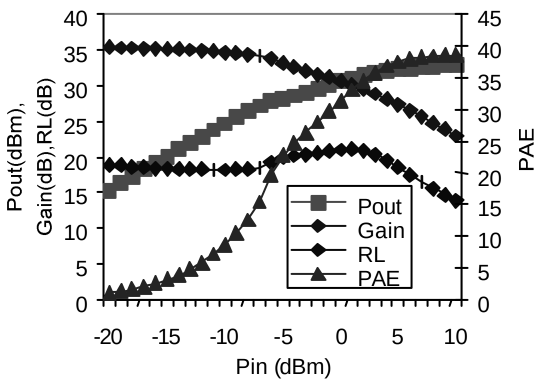

Fig. 6. Pout, Gain, Input Return Loss and PAE versus Pin for DCS power amplifier under 3.2V at 1800 MHz

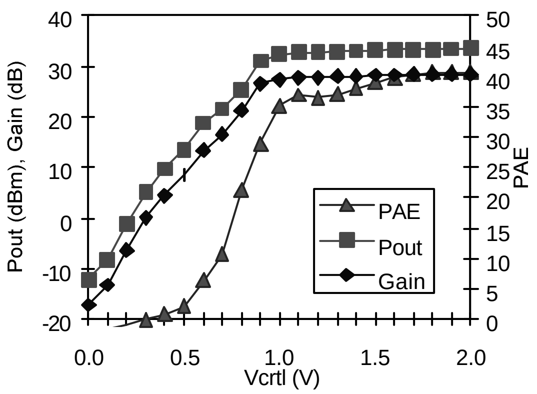

Fig. 7. Pout, Gain and PAE as a function of Power Control Voltage for DCS power amplifier under 3.2V and Pin=5dBm at 1800MHz.

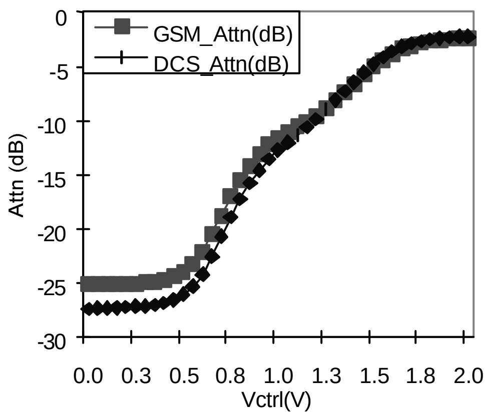

Fig. 8. the attenuation of Voltage Control Attenuator as a function of Power Control Voltage for GSM and DCS power amplifiers and Pin=5dBm

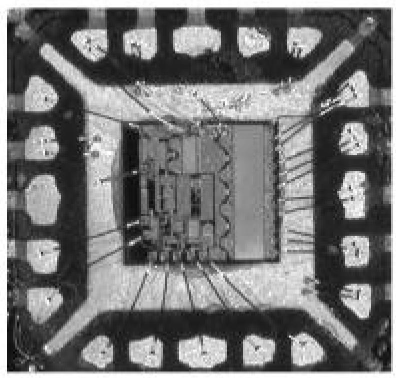

Fig. 9. The photograph of the assembled DCS PA

IV. CONCLUSION

In conclusion, small chip size GSM and DCS power amplifiers, housed in MLP20 packages, have been developed for low voltage wireless applications using a newly developed 0.5um enhancement mode power PHEMT process. On the evaluation board the GSM PA provides greater than +35 dBm with 55% PAE, and the DCS PA delivers greater than +33dBm with 40% PAE, both using a single power supply of 3.2V. Note that this performance is achieved in a tiny plastic leadless package, MLP20, which occupies only 4mm$\times$4 mm on board.

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